What is claimed is:

1. A data encoder for encoding a codeword having a plurality of symbols for transmission through a data channel, the data encoder comprising:

a turbo encoder having:

an interleaver for receiving the codeword and providing an interleaved codeword;

first and second recursive systematic convolutional (RSC) encoders, the first RSC encoder for receiving the codeword and providing first parity bits in accordance with the codeword, the second RSC encoder for receiving the interleaved codeword from the interleaver and providing second parity bits in accordance with the interleaved codeword;

a puncturer for receiving the codeword, the first parity bits and the second parity bits, and for puncturing at least the first and second parity bits in accordance with a pattern of a desired code rate; and

a mapper for receiving the punctured parity bits, and for providing signal sets in accordance with the desired code rate.

2. The data encoder of claim 1, wherein the interleaver is a modified dithered relatively prime interleaver.

3. The data encoder of claim 1, wherein the first and second RSC encoders are rate 2/3, 8 state RSC encoders.

4. The data encoder of claim 3, further including a Reed-Solomon encoder for encoding the codeword prior to receipt by the turbo encoder.

5. The data encoder of claim 4, further including a Forney interleaver disposed between the Reed-Solomon encoder and the turbo encoder, for interleaving the symbols in the codeword prior to receipt by the turbo encoder.

6. The data encoder of claim 3, wherein the codeword is a 25600-bit frame.

7. The data encoder of claim 6, wherein the RSC encoders employ tail-biting termination, and polynomials of the each of the first and second RSC encoders are chosen such that for a final state of a first pass through the RSC encoder having bit positions [0 1 2 3 4 5 6 7], a final state of a second pass through the RSC encoder yields bit positions [0 5 1 4 2 7 3 6].

8. The data encoder of claim 1, wherein the turbo encoder includes a further interleaver coupled to a further RSC encoder, the further interleaver receiving the codeword and providing a further interleaved codeword to the further RSC encoder, the further RSC encoder providing further parity bits to the puncturer.

9. A turbo encoder system for encoding a digital signal including a codeword having a plurality of symbols, comprising:

a Reed-Solomon encoder, for receiving and encoding the codeword;

a Forney interleaver, for receiving from the Reed Solomon encoder, the encoded codeword, and for interleaving the symbols in the codeword according to a predetermined interleaver index; and

a turbo encoder for receiving the interleaved encoded codeword from the Forney interleaver, the turbo encoder having at least one modified dithered relatively prime interleaver for interleaving the codeword, at least two RSC encoders for encoding the codeword and the interleaved codeword, respectively, and a puncturer for puncturing the codeword, the encoded codeword, and the interleaved and encoded codeword to provide a turbo codeword.

10. The turbo encoder system of claim 9, wherein the at least two RSC encoders are rate 2/3, 8 state RSC encoders using tail-biting termination.

11. The turbo encoder system of claim 10, wherein for a 25600-bit codeword, polynomials of the at least two RSC encoders are chosen such that for a final state of a first pass through the RSC encoder having bit positions [0 1 2 3 4 5 6 7], a final state of a second pass through the RSC encoder yields bit positions [0 5 1 4 2 7 3 6].

12. A turbo coding method, comprising the steps of:

encoding a plurality of codewords according to a Reed-Solomon (RS) outer code;

interleaving the plurality of RS encoded codewords;

providing each of the plurality of interleaved codewords to a first RSC encoder for encoding using a systematic recursive convolutional constituent (RSCC) code to provide first parity bits;

providing each of the plurality of interleaved codewords to an interleaver coupled to a second RSC encoder for interleaving each codeword and for encoding each doubly interleaved codeword using a RSCC code to provide second parity bits;

puncturing the first and second parity bits in accordance with a pattern of a desired code rate; and

mapping the punctured parity bits to provide signal sets in accordance with the desired code rate.

13. The turbo coding method of claim 12, wherein the RSCC code is a rate 2/3, 8 state RSCC code.

14. The turbo encoding method of claim 13, wherein for a digital signal which is a 25600-bit frame, RSCC polynomials are chosen such that for a final state of a first pass through the RSC encoder having bit positions [0 1 2 3 4 5 6 7], a final state of a second pass through the RSC encoder yields bit positions [0 5 1 4 2 7 3 6].

15. The turbo coding method of claim 12, wherein the interleaving of the plurality of RS encoded codewords uses a Forney interleaver.

16. The turbo coding method of claim 12, wherein the interleaving of each of the plurality of RS encoded codewords consists of interleaving using a modified dithered relatively prime interleaving mapping.

17. The turbo coding method of claim 12, further including the steps of transmitting the signal sets, receiving the transmitted signal set, and decoding the signal set using standard log-maximum-a-posteriori-probability (log-MAP) decoding.

18. The turbo coding method of claim 17, wherein the decoding further includes early stopping.